REMARKS

Claims 1 to 3 and 10 to 13 were pending in the present application. Applicant has amended claims 1, 2, and 10 to 12. Claims 1 to 3 and 10 to 13 remain pending.

§ 112 Rejections

The Examiner rejected claim 12 under 35 U.S.C. § 112, first paragraph, for introducing new matter. Specifically, the Examiner found that "[n]owhere in the original disclosure is there support for writing new data into a line of memory, reading existing data from the line of memory, merging the written new data with the existing data, and writing again to the line of memory the merged data." August 15, 2007 Office Action, p. 3. The Examiner then rejected claims 1 and 12 under 35 U.S.C. § 112, second paragraph, as being indefinite. Specifically, the Examiner found it "is unclear whether an 'entire line of memory' is a physical word line of a memory, or whether it is series of fixed consecutive memory addresses.'" Id. The Examiner then found "it unclear whether mirroring a write comprises the steps of claim 1; or whether it comprises the steps of claim 12." Id., p. 4.

Applicant has amended claims 1 and 12 to clarify the claim language. Amendments to claims 1 and 12 are supported by the Specification at p. 13, lines 15 to 24 and p. 28, line 4 to p. 29, line 23.

Applicant submits that a "line of memory" is the basic unit of memory operation. In other words, the cluster memory is read and written in the units of an N-byte line. For example, a 64-byte line of memory is access through a burst of 8 consecutive 64-bit pieces of memory.

§ 103 Rejections of Claims 1 to 3 and 10, 12, and 13

The Examiner rejected claims 1 to 3, 10, 12, and 13 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,049,889 ("Steely, Jr. et al.") in view of U.S. Patent No. 5,850,556 ("Grivna"), and further in view of U.S. Patent No. 5,887,134 ("Ebrahim").

Claim 1

Addressing Applicant's argument that the cited references do not disclose a memory copy write command that copies an entire line of memory from a local node to a remote node even when the line is only partially written with new data, the Examiner stated:

> Steely teaches in col. 4, lines 54-57 that the memory address space is divided into N pages of data, where each page is 8 kilobytes of data. Therefore, it is clear that data must be transmitted in pages of 8k bytes because Steely states that "connection granularity between nodes in the network is at the page level". When data smaller than 8k bytes is written into the memory address space, the entire 8k bytes of data must be transmitted because that is the page size as indicated by Steely).

August 15, 2007 Office Action, p. 6. Applicant respectfully traverses.

Steely et al. does not disclose or suggest that an entire page at a node is mirrored to another node when less than the entire page is written. Steely et al. only discloses that the PCI address space 47 at a node is divided into pages and each page is assigned ("connected") to one or more nodes in the system.

> Thus, connection granularity between nodes in the network is at the page level. Certain nodes in the network will receive data when the CPU writes to one of the N pages of MC address space. The determination of which nodes are mapped to which network addresses, i.e. the mapped connection, are determined at some point prior to when the nodes require data transfer.

Steely et al. col. 4, lines 56 to 64 (emphasis added). Connection granularity simply refers to the correspondence between pages and nodes. For at least this reason, claim 1 is patentable over the combination of Steely Jr. et al., Grivna, and Ebrahim.

Claims 2, 3, 10, and 12 to 13

Claims 2, 3, 10, and 12 to 13 depend from claim 1 and are patentable over the cited references for at least the same reasons as claim 1.

§ 103 Rejection of Claim 11

The Examiner rejected claim 11 as being unpatentable over Steely et al. in view of Grivna and Ebrahim as applied to claim 1, and further in view of U.S. Patent No. 5,914,970 ("Gunsaulus et al."). Specifically, the Examiner found that Steely et al., Grivna, and Ebrahim do not disclose computing parity over multiple blocks of data from a local memory at a local node and writing the parity to a remote memory of a remote node. The Examiner then cited Gunsaulus et al. for disclosing computing parity for a number of memory devices and writing the parity to a memory device, and found it to be obvious to modify the combination of Steely et al., Grivan, and Ebrahim with Bhunsaulus et al. because "one of ordinary skill in the art would have recognized that using one

memory device for parity storage reduces the number of memory devices needed for storing parity, as disclosed by Gunsaulus in col. 1, lines 52-55." August 15, 2007 Office Action, p. 9. Applicant respectfully traverses.

The Examiner misunderstood the invention of claim 11. Claim 11 recites a DMA operation that replaces what would have been two or more operations in the prior art.

> In one embodiment, for a DMA engine write, rather than copying data from a local memory location to a remote memory location, the data that is written to the remote node 14 can be computed, for example, by computing parity over multiple blocks of data on the local node 14. This can eliminate one entire operation in some cases. That is, if the same function was to be performed in previously developed systems, parity of the local blocks must first be calculated and then saved in local memory. Next, the computed parity from local memory is transferred (as a DMA operation) to the remote node as a separate operation. With the communication for DMA engine write (in accordance with an embodiment of the present invention, parity of the local blocks can be calculated (or computed) and transferred (as a DMA operation) to the remote node, thus saving an extra write operation to memory and an extra read operation from memory.

Specification, p. 12, line 25 to p. 13, line 14. Thus, the invention of claim 11 is simply not the storing of parity for multiple blocks of data into a single memory device as suggested by the Examiner. Instead, the invention combines parity calculation and DMA transfer into one single operation, which is not disclosed or suggested by the cited references either alone or in combination. For at least this reason, claim 11 is patentable over the cited references.

Summary

In summary, claims 1 to 3 and 10 to 13 were pending in the present application. Applicant has amended claims 1, 2, and 10 to 12. Applicant requests the Examiner to withdraw his claim objection/rejections and allow claims 1 to 3 and 10 to 13. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

Respectfully submitted,

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